

WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device including a memory cell array of non-volatile memory cells arranged in rows and columns, each row having a word line and a plate line, comprising:

5 a pulse generator circuit capable of generating a pulse signal responsive to an address;
a chip enable buffer circuit capable of activating a chip enable flag signal responsive to the pulse signal;

a row selector circuit capable of selecting a row responsive to the address and the chip enable flag signal and capable of generating a plate flag signal associated with a plate line of
10 the selected row; and

a control circuit capable of generating a plate control signal responsive to a write enable signal and the pulse signal;

where the row selector circuit is capable of activating the plate line responsive to the plate control signal.

15 2. The memory device of claim 1 comprising a sense amplifier circuit capable of sensing and amplifying data responsive to a sense amplification enable signal.

3. The memory device of claim 2
20 where the control circuit is capable of activating the sense amplification enable signal responsive to the plate flag signal; and

where the control circuit is capable of deactivating the sense amplification enable signal responsive to the pulse signal.

25 4. The memory device of claim 2
where the chip enable buffer circuit is capable of deactivating the chip enable flag signal responsive to deactivation of the sense amplification enable signal.

5. The memory device of claim 1
30 where a word line of the selected row is deactivated in synchronization with the chip enable flag signal.

6. The memory device of claim 1
where the plate flag signal is active for a predetermined time; and
where the plate line is driven during the predetermined time.

5 7. The memory device of claim 2
where the activated sense amplification enable signal is deactivated after a plate line
is deactivated.

8. A memory device, comprising:
10 a memory cell array having non-volatile memory cells arranged in rows and columns,
each row comprising at least one word line and one plate line;
a pulse generator circuit capable of generating a pulse signal responsive to a transition
of an address;
a chip enable buffer circuit capable of buffering an external chip enable signal and
15 activating a chip enable flag signal responsive to a first transition of the pulse signal;
a row selector circuit capable of selecting a row responsive to the address and capable
of generating a flag signal associated with a plate line; and
a control circuit capable of activating a plate control signal responsive to activation of
a write enable signal and deactivating the plate control signal responsive to a second
20 transition of the pulse signal;
where the row selector circuit is capable of activating a plate line associated with the
selected row responsive to the plate control signal; and
where the pulse generator circuit is capable of generating the pulse signal responsive
to the external chip enable signal when the external chip enable signal transitions in the
25 absence of an address transition.

9. The memory device of claim 8 comprising a sense amplifier circuit capable of
sensing and amplifying data from the selected row and columns responsive to a sense
amplification enable signal.

30 10. The memory device of claim 9
where the control circuit is capable of activating the sense amplification enable signal
responsive to the flag signal; and

where the control circuit is capable of deactivating the sense amplification enable signal responsive to the second transition of the pulse signal.

11. The memory device of claim 9

5 where the chip enable buffer circuit is capable of deactivating the chip enable flag signal responsive to deactivation of the sense amplification enable signal.

12. The memory device of claim 8

10 where a word line of the selected row is deactivated in synchronization with the chip enable flag signal.

13. The memory device of claim 8

15 where the flag signal is a pulse signal activated for a predetermined time and a plate line of the selected row is driven during an active period of the pulse signal.

14. The memory device of claim 9

where the sense amplification enable signal is deactivated after a plate line is deactivated.

20 15. A non-volatile semiconductor memory device including a plurality of word lines, a plurality of plate lines corresponding to the word lines, a plurality of bit lines, and a plurality of ferroelectric memory cells, comprising:

a row address latch circuit capable of latching a row address responsive to a chip enable flag signal;

25 a column address latch circuit capable of latching a column address responsive to the chip enable flag signal;

a pulse generator circuit capable of generating a pulse signal responsive to the row and column addresses;

30 a chip enable buffer circuit capable of buffering an external chip enable signal and of activating the chip enable flag signal responsive to the pulse signal;

a row selector circuit capable of selecting a word line and a plate line associated with the selected word line responsive to the address and to the chip enable flag signal and of generating a plate flag signal selecting a plate line; and

a sense amplifier circuit capable of sensing and amplifying data from the selected word line responsive to a sense amplification enable signal;

a control circuit capable of activating the sense amplification enable signal responsive to the flag signal and of deactivating the sense amplification enable signal responsive to the pulse signal;

where the control circuit is capable of activating a plate control signal responsive to a write enable signal and of deactivating the plate control signal responsive to the pulse signal; and

where the row selector circuit is capable of activating a plate line associated with the selected word line responsive to activation of the plate control signal and of deactivating the plate line associated with the selected word line responsive to deactivation of the plate control signal.

16. The memory device of claim 15

where the pulse generator circuit is capable of generating the pulse signal responsive to the external chip enable signal when the external chip enable signal transitions in the absence of an address transition.

17. The memory device of claim 15 comprising:

a column selector circuit capable of selecting at least one of the bit lines responsive to the column address; and

a data input/output circuit capable of outputting sensed data corresponding to the selected bit lines during a read operation and of transferring write data to the selected bit lines during a write operation.

18. The memory device of claim 15

where the chip enable buffer circuit is capable of deactivating the chip enable flag signal responsive to deactivation of the sense amplification enable signal.

19. The memory device of claim 15

where the selected word line is deactivated in synchronization with the chip enable flag signal.

20. The memory device of claim 15
where the flag signal is a pulse signal activated for a predetermined time; and
where the selected plate line is driven during an activation period of the pulse signal.

5 21. The memory device of claim 15
where the sense amplification enable signal is deactivated after a plate line is
deactivated.

22. A method for controlling a non-volatile semiconductor memory device
10 including a plurality of word lines, a plurality of plate lines corresponding to the word lines, a
plurality of bit lines, and a plurality of ferroelectric memory cells, the method comprising:
generating a pulse signal responsive to a first transition of an address;
activating the word line and plate line corresponding to the address responsive to the
pulse signal;
15 deactivating the plate line after a predetermined time; and
activating the plate line responsive to a write enable signal in the absence of an
address transition.

23. The method of claim 22 comprising deactivating the plate line using a plate
20 signal responsive to the address.

24. The method of claim 22 comprising activating the write enable signal
substantially simultaneously with activating the plate line.

25 25. The method of claim 22 comprising activating the write enable signal after
deactivating the plate line.

26. A method for controlling a non-volatile semiconductor memory device
including a memory cell array having a plurality of word lines, a plurality of plate lines
30 corresponding to the word lines, a plurality of bit lines, a plurality of ferroelectric memory
cells, and a sense amplifier circuit for sensing and amplifying data from the memory cell
array, the method comprising:
generating a pulse signal responsive to a first address transition;

activating a word line and a plate line corresponding to the address responsive to a first transition of the pulse signal:

deactivating the plate line after a predetermined time;

activating the sense amplifier circuit responsive to activation of the plate line; and

5 sequentially deactivating the sense amplifier circuit and the word line responsive to a second transition of the pulse signal, the second transition of the pulse signal being generated responsive to a second address transition.

27. The method of claim 26 comprising activating the word line and the plate line
10 before activating the sense amplifier circuit.

28. The method of claim 26 comprising generating the pulse signal responsive to the chip enable signal, the chip enable signal transitioning in the absence of an address transition.

15 29. The method of claim 26 comprising latching an address responsive to a chip enable flag signal, the chip enable flag signal activating responsive to the first transition of the pulse signal and deactivating responsive to the sense amplifier circuit.

20 30. A method for controlling a non-volatile semiconductor memory device including a memory cell array having a plurality of word lines, a plurality of plate lines corresponding to the word lines, a plurality of bit lines, a plurality of ferroelectric memory cells, and a sense amplifier circuit for sensing and amplifying data from the memory cell array, the method comprising:

25 generating a pulse signal responsive to a first transition of an address;

activating a word line and a plate line associated with the address responsive to the pulse signal;

deactivating the plate line after a predetermined time;

activating the sense amplifier circuit responsive to activation of the plate line; and

30 re-activating the plate line responsive to activation of a write enable signal in the absence of an address transition.

31. The method of claim 30 comprising deactivating the sense amplifier circuit responsive to a second transition of the address.

32. The method of claim 31 comprising deactivating the word line responsive to deactivating the sense amplifier circuit.

5 33. The method of claim 30 comprising activating the write enable signal substantially simultaneously with activating the plate line.

34. The method of claim 30 comprising activating the write enable signal after deactivating the plate line.

10 35. The method of claim 30 comprising latching an address responsive to a chip enable flag signal, the chip enable flag signal activating responsive to the pulse signal and deactivating responsive to deactivating the sense amplifier circuit.